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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,800	04/02/2004	Yoshito Date	60188-813	9354

7590 08/10/2005

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER

TON, MY TRANG

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/815,800	Applicant(s) DATE ET AL.	
	Examiner My-Trang N. Ton	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

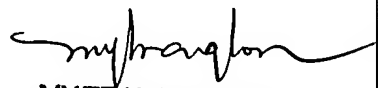
Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.


MY-TRANG N. TON
PRIMARY EXAMINER

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>4/2/04</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, the limitation “the second current distribution MISFET and the first current distribution MISFET constituting a current mirror circuit” (lines 19-20) is misdescriptive of the present invention since such limitation is not seen as recited therein (if considered transistor 2 as the first current distribution and transistor 6 as second current distribution). In order to avoid any confusion, Applicant is required to particularly point out how this limitation reads on the circuit arrangement of the drawings. If considered the first current distribution MISFET as transistor 1 and the second current distribution MISFET as transistor 2 then the limitation “a drain of the second current distribution MISFET being connected to the drain of the second current input MISFET (7) is misdescriptive. Similar problem occurs for “the third current distribution MISFET ... and the second current distribution MISFET constituting a current mirror circuit” (lines 22-24).

Claim 4 is similarly rejected as claim 1 regarding the limitation “the additional current distribution MISFET, the second current distribution MISFET and the third current distribution MISFET constituting a current mirror”.

Claim 9 is similarly rejected as above claims regarding the limitation “the second current distribution MISFET and the first current distribution MISFET constituting a current mirror”.

Claim 10 is also similarly rejected as above claims regarding the limitation “the third current input MISFET and the first current input MISFET constituting a current mirror circuit”.

In claim 12, the limitation “a gate electrode of the current output MISFET being connected between the gate electrode of the first current input MISFET and the gate electrodes of the current source MISFETs” (lines 2-4) is misdescriptive of the present invention since such limitation is not seen as recited therein. In order to avoid any confusion, Applicant is required to particularly point out how this limitation reads on the circuit arrangement of the drawings. Moreover, it is not fully clear which element is referred as “a third current distribution MISFET” and “a fourth current distribution MISFET” as recited in claim 12.

Regarding claim 13, it is not fully clear which element is referred as “a fifth current distribution MISFET” as recited.

In claim 14, the limitation “a current-voltage converter ... from the second current distribution MISFET by 200Mm or less” (lines 20-23) is misdescriptive of the present invention since such limitation is not seen as recited therein. In order to avoid any confusion, Applicant is required to particularly point out how this limitation reads on the circuit arrangement of the drawings.

Claim 19 is similarly rejected as claim 1 regarding the limitation “the second current distribution MISFET and the first current distribution MISFET constituting a current mirror circuit” (lines 22-23) and “the third current distribution MISFET, the first current distribution MISFET and the second current distribution MISFET constituting a current mirror circuit” (lines 27-28).

Claims 2-3, 5-7, 11, 15-18, 20-21 are rendered indefinite by the deficiencies of above claims.

Claim 22 is similarly rejected as claim 4 regarding the limitation “the additional current distribution MISFET, the second current distribution MISFET and the third current distribution MISFET constituting a current mirror” (lines 5-7). Furthermore, it is unclear which element is referred as “a fifth current input MISFET” as recited in claim 22.

In claim 23, the limitation “a first current-voltage converter ... which is distant from the second current distribution MISFET by 200Mm or less” (lines 24-27) is misdescriptive of the present invention since such limitation is not seen as recited therein. In order to avoid any confusion, Applicant is required to particularly point out how this limitation reads on the circuit arrangement of the drawings. Also, it is unclear which element is referred as “a third current distribution MISFET” as recited in line 35.

Claim 24 is similarly rejected as claim 23 regarding limitation “a first current-voltage converter”, “a first load circuit”, “a second load circuit” and “a second current-voltage converter”.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by the prior art depicted by Applicant's Fig. 14.

The prior art, Fig. 14 discloses a conventional current driver including:

a first current input terminal (connected to 1109);

a first current input MISFET (1110) of a first conductivity type, a drain of the first current input MISFET (1110) being connected to the first current input terminal, and the drain and gate electrode of the first current input MISFET (1110) being connected to each other;

a plurality of current supply sections (1112-1 – 1112-n) including current source MISFETS (1112-1 – 1112-n) of the first conductivity type (n type), the current source MISFETS (1112-1 – 1112-n) and the first current input MISFET (1110) constituting a current mirror circuit, and

a bias line (line connected to gate of 1110, 1112-1 – 1112-n) which is commonly connected to the gate electrode of the first current input MISFET (1110) and the gate electrodes of the current source MISFETS (1112-1 – 1112-n) as recited in claim 8.

Art Unit: 2816

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



My-Trang N. Ton
Primary Examiner
Art Unit 2816

August 4, 2004